20. (New) A data transmission method comprising:

setting a first power margin;

measuring a plurality of signal-to-noise ratios associated with a plurality of sub-channels;

determining a plurality of data capacities associated with the sub-channels at the first power margin, wherein the data capacities are determined through calculating a plurality of bit loadings associated with the sub-channels at the first power margin;

determining a plurality of power modification factors corresponding to the bit loadings at the first power margin;

calculating a first total bit rate according to the data capacities; and

adjusting the first total bit rate to meet a target data rate through adjusting the data capacities, wherein the data capacities are adjusted according to the bit loadings and the power modification factors.

21. (New) The method of claim 20, further comprising verifying the bit loadings and the power modification factors at the first power margin.

22. (New) The method of claim 20, wherein the power modification factors are determined according to at least one of the signal-to-noise ratios and a plurality of bit error rates associated with the sub-channels.

23. (New) The method of claim 20, where the bit loadings associated with each of the sub-channels include a first bit number and a second bit number, wherein the first

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bit number is larger than the second bit number, and the power modification factors associated with each of the sub-channels include a first power factor corresponding to the first bit number and a second power modification factor corresponding to the second bit number.

24. (New) The method of claim 23, wherein the data capacities are adjusted sequentially in an order determined according to the first power factor, the second power factor, the first bit number, and the second bit number associated with each of the sub-channels.

25. (New) The method of claim 24, wherein the first bit number of bit loadings of one of the sub-channels is a data capacity of the sub-channel.

26. (New) The method of claim 25, wherein the order is a descending order according to the difference between the first power factor and the second power factor divided by the difference between the first bit number and the second bit number associated with each of the sub-channels.

27. (New) The method of claim 26, wherein the data capacity associated with one of the sub-channels is adjusted through substituting the first power factor with the second power factor and substituting the first bit number with the second bit number associated with the channel.

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28. (New) The method of claim 23, wherein the first bit number is a maximum bit loading and the second bit number is a minimum bit loading associated with each of the sub-channels.

29. (New) The method of claim 28, wherein the data capacities are adjusted sequentially in an order determined according to a plurality of power adjustment values associated with the sub-channels, wherein the power adjustment values are determined by the following equation:

(emax(i)-emin(i))/(bmax(i)-bmin(i))

where bmin(i) and bmax(i) respectively are the minimum and maximum bit loadings for each of the sub-channels, and emin(i) and emax(i) respectively are the first and second power factors respectively associated with the minimum and the maximum bit loading.

30. (New) The method of claim 29, wherein the maximum bit loading of each sub-channel is a maximum data capacity associated with the sub-channel.

31. (New) The method of claim 20, further comprising determining whether to enable or disable each of the sub-channels according to the bit loadings and the power modification factors.

32. (New) The method of claim 20, wherein the method further comprising:

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determining a second power margin according to the difference between the first total bit rate and the target data rate after adjusting the first total bit rate;

calculating a second total bit rate at the second power margin according to the data capacities associated with the sub-channels at the second power margin; and

adjusting the second total bit rate through adjusting the data capacities associated with the sub-channels at the second power margin,

wherein the difference between the second total bit rate and the target data rate is smaller than the difference between the first total bit rate and the target data rate.

33. (New) The method of claim 32, further comprising verifying the bit loadings and the power modification factors at the second power margin.

34. (New) The method of claim 32, wherein when the target bit rate is between the first total bit rate and the second total bit rate, the method further comprises:

determining a third power margin according to the first power margin and the second power margin, wherein the third power margin is between the first power margin and the second power margin; and

calculating a third total bit rate at the third power margin according to the data capacities associated with the sub-channels at the third power margin,

wherein the difference between the third total bit rate and the target data rate is smaller than the difference between the second total bit rate and the target data rate.

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35. (New) The method of claim 32, wherein the third power margin is the square root of the multiplication of the first power margin and the second power margin.

36. (New) The method of claim 20, wherein the data capacities are determined and adjusted according to at least one of changes in communication system characteristics and changes in the target data rate.

37. (New) The method of claim 36, wherein the communication system characteristics include the signal-to-noise ratios associated with the sub-channels.

38. (New) The method of claim 20, wherein the data capacities are determined and adjusted through considering a maximum transmission power of a communication system.

39. (New) A method of controlling data transmission comprising:

measuring a plurality of signal-to-noise ratios associated with a plurality of sub-channels;

calculating a plurality of data capacities associated with the sub-channels according to the signal-to-noise ratios; and

calculating a total bit rate according to the data capacities; and

when a target data rate is larger than the total bit rate,

calculating a plurality of first power margin factors associated with the sub-channels, wherein each of the first power margin factors represents a power

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margin factor of a sub-channel when at least one additional bit is added to the sub-channel; and

allocating at least one bit to at least one of the sub-channels according to the first power margin factors associated with the sub-channels.

40. (New) The method of claim 39, further comprising repeating the steps of calculating the first power margin factors and allocating bits until the total bit rate approximates or equals to the target data rate.

41. (New) The method of claim 39, wherein the first power modification factors are determined according to at least one of the signal-to-noise ratios and a plurality of bit error rates associated with the sub-channels.

42. (New) The method of claim 39, wherein the additional bits are allocated to the sub-channels in an order based on the first power margin factors.

43. (New) The method of claim 42, wherein the order is a descending order based on the value of the first power margin factor associated with each of the sub-channels.

44. (New) The method of claim 39, wherein when the target data rate is smaller than the total bit rate, the method further comprises:

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calculating a plurality of second power margin factors associated with the sub-channels, wherein each of the second power margin factors represents a power margin factor of a sub-channel when at least one bit is removed from the sub-channel; and

dropping at least one unused bit from at least one of the sub-channels according to the second power margin factors associated with the sub-channels.

45. (New) The method of claim 44, further comprising repeating the steps of calculating the second power margin factors and dropping bits until the total bit rate approximates or equals to the target data rate.

46. (New) The method of claim 44, wherein the second power margin factors are determined according to at least one of the signal-to-noise ratios and a plurality of bit error rates associated with the sub-channels.

47. (New) The method of claim 44, wherein the at least one unused bit is dropped from at least one of the sub-channels in an order based on the second power margin factors.

48. (New) The method of claim 44, wherein the order is an ascending order based on the value of the second power margin factor associated with each of the sub-channels.

49. (New) A method for transmitting data through sub-channels, comprising:

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providing a power margin;

obtaining signal-to-noise ratios associated with the sub-channels;

determining bit loading capacities and power modification factors associated with the sub-channels at the power margin; and

determining a total bit rate at the power margin according to at least one of the bit loading capacities and power modification factors.

50. (New) The method of claim 49, further comprising verifying the bit loadings and the power modification factors at the power margin.

51. (New) The method of claim 49, further comprising:

providing a target bit rate;

determining an estimated power margin according to at least one of the total bit rate and the target bit rate;

replacing the power margin with the estimated power margin;

repeating, as a first loop, the steps of determining the bit loading capacities and the power modification factors, of determining the total bit rate, of determining the estimated power margin, and of replacing the power margin, for a predetermined number of times, until the total bit rate approximates or equals to the target bit rate, or until obtaining two total bit rates that bound the target bit rate between the two total bit rates.

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52. (New) The method of claim 51, when obtaining two total bit rates that bound the target bit rate between the two total bit rates, the method further comprises:

determining an updated power margin according to the two estimated power margins associated with the two total bit rates;

replacing the power margin with the updated power margin;

repeating the first loop until obtaining the two total bit rates that bound the target bit rate and the steps of determining the updated power margin according to the two estimated power margins associated with the two total bit rates and of replacing the power margin with the updated power margin, for a predetermined number of times or until a most recent total bit rate approximates or equals to the target bit rate.

53. (New) The method of claim 52, wherein the updated power margin is the square root of the multiplication of the two estimated power margins associated with the two total bit rates.

54. (New) The method of claim 49, wherein determining the bit loading capacities and the power modification factors comprising determining the bit loading capacities and the power modification factors according to at least one of the signal-to-noise ratios, data rates associated with the sub-channels, number of sub-channels having a non-zero bit capacity, and a system transmission power.

55. (New) The method of claim 49, wherein the bit loading capacity of each sub-channel is represented by a minimum bit loading and a maximum bit loading.

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56. (New) The method of claim 49, wherein each sub-channel has a minimum power modification factor and a maximum power modification factor respectively associated with the minimum bit loading and the maximum bit loading.

57. (New) The method of claim 49, wherein obtaining the signal-to-noise ratios includes using previously existed signal-to-noise ratios as the signal-to-noise ratios or measuring updated signal-to-noise ratios as the signal-to-noise ratios.

58. (New) The method of claim 49, further comprising determining whether to enable or disable at least one of the sub-channels according to the bit loadings and the power modification factors.

59. (New) A data transmission system comprising:

a memory to store a plurality of signal-to-noise ratios associated with a plurality of sub-channels; and

a processor configured to

determine a plurality of data capacities associated with the sub-channels at a first power margin, wherein the data capacities are determined through calculating a plurality of bit loadings associated with the sub-channels at the first power margin;

determine a plurality of power modification factors corresponding to the bit loadings at the first power margin;

calculate a first total bit rate according to the data capacities; and

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adjust the first total bit rate to meet a target data rate through adjusting the data capacities, wherein the data capacities are adjusted according to the bit loadings and the power modification factors.

60. (New) The system of claim 59, wherein the processor is configured to verify the bit loading and the power modification factors at the first power margin.

61. (New) The system of claim 59, wherein the power modification factors are determined according to at least one of the signal-to-noise ratios and a plurality of bit error rates associated with the sub-channels.

62. (New) The system of claim 59, where the bit loadings associated with each of the sub-channels include a first bit number and a second bit number, wherein the first bit number is larger than the second bit number, and the power modification factors associated with each of the sub-channels include a first power factor corresponding to the first bit number and a second power modification factor corresponding to the second bit number.

63. (New) The system of claim 62, wherein the data capacities are adjusted sequentially in an order determined according to the first power factor, the second power factor, the first bit number, and the second bit number associated with each of the sub-channels.

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64. (New) The system of claim 63, wherein the first bit number of bit loadings of one of the sub-channels is a data capacity of the sub-channel.

65. (New) The system of claim 64, wherein the order is a descending order according to the difference between the first power factor and the second power factor divided by the difference between the first bit number and the second bit number associated with each of the sub-channels.

66. (New) The system of claim 65, wherein the data capacity associated with one of the sub-channels is adjusted through substituting the first power factor with the second power factor and substituting the first bit number with the second bit number associated with the channel.

67. (New) The system of claim 62, wherein the first bit number is a maximum bit loading and the second bit number is a minimum bit loading associated with each of the sub-channels.

68. (New) The system of claim 67, wherein the data capacities are adjusted sequentially in an order determined according to a plurality of power adjustment values associated with the sub-channels, wherein the power adjustment values are determined by the following equation:

(emax(i)-emin(i))/(bmax(i)-bmin(i))

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where bmin(i) and bmax(i) respectively are the minimum and maximum bit loadings for each of the sub-channels, and emin(i) and emax(i) respectively are the first and second power factors respectively associated with the minimum and the maximum bit loading.

69. (New) The system of claim 68, wherein the maximum bit loading of each sub-channel is the maximum data capacity associated with the sub-channel.

70. (New) The system of claim 59, where in the processor is configured to determine whether to enable or disable each of the sub-channels according to the bit loadings and the power modification factors.

71. (New) The system of claim 59, wherein the processor is configured to

determine a second power margin according to the difference between the first total bit rate and the target data rate;

calculate a second total bit rate at the second power margin according to the data capacities associated with the sub-channels at the second power margin; and

adjust the second total bit rate through adjusting the data capacities,

wherein the difference between the second total bit rate and the target data rate is smaller than the difference between the first total bit rate and the target data rate.

72. (New) The system of claim 71, wherein the processor is configured to verify the bit loading and the power modification factors at the second power margin.

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73. (New) The system of claim 71, wherein when the target bit rate is between the first total bit rate and the second total bit rate, the processor is configured to

determine a third power margin according to the first power margin and the second power margin, wherein the third power margin is between the first power margin and the second power margin; and

calculate a third total bit rate at the third power margin according to the data capacities associated with the sub-channels at the third power margin,

wherein the difference between the third total bit rate and the target data rate is smaller than the difference between the second total bit rate and the target data rate.

74. (New) The system of claim 73, wherein the third power margin is the square root of the multiplication of the first power margin and the second power margin.

75. (New) The system of claim 59, wherein the data capacities are determined and adjusted according to at least one of changes in communication system characteristics and changes in the target data rate.

76. (New) The system of claim 75, wherein the communication system characteristics include the signal-to-noise ratios associated with the sub-channels.

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77. (New) The system of claim 59, wherein the data capacities are determined and adjusted through considering a maximum transmission power of a communication system.

78. (New) A system of controlling data transmission comprising:

a memory to store a plurality of signal-to-noise ratios associated with a plurality of sub-channels; and

a processor configured to

calculate a plurality of data capacities associated with the sub-channels according to the signal-to-noise ratios; and

calculate a total bit rate according to the data capacities; and

when a target data rate is larger than the total bit rate, the processor is configured to

calculate a plurality of first power margin factors associated with the sub-channels, wherein each of the first power margin factors represents a power margin factor of a sub-channel when at least one bit is added to the sub-channel; and

allocate at least one additional bit to at one of the sub-channels according to the first power margin factors associated with the sub-channels.

79. (New) The system of claim 78, the processor is configured to repeat the steps of calculating the first power margin factors and to allocate the additional bits until the total bit rate approximates or equals to the target data rate.

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80. (New) The system of claim 78, wherein the first power modification factors are determined according to at least one of the signal-to-noise ratios and a plurality of bit error rates associated with the sub-channels.

81. (New) The system of claim 78, wherein the additional bits are allocated to the sub-channels in an order based on the first power margin factors.

82. (New) The system of claim 81, wherein the order is a descending order based on the value of the first power margin factor associated with each of the sub-channels.

83. (New) The system of claim 78, wherein when the target data rate is smaller than the total bit rate, the processor is configured to

calculate a plurality of second power margin factors associated with the sub-channels, wherein each of the second power margin factors represents a power margin factor of a sub-channel when at least one bit is removed from the sub-channel; and

drop at least one unused bit from at least one of the sub-channels according to the second power margin factors associated with the sub-channels.

84. (New) The system of claim 83, wherein the second power modification factors are determined according to at least one of the signal-to-noise ratios and a plurality of bit error rates associated with the sub-channels.

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85. (New) The system of claim 83, wherein the processor is configured to repeat the steps of calculating the second power margin factors and to drop the at least one unused bit until the total bit rate approximates or equals to the target data rate.

86. (New) The system of claim 85, wherein the at least one unused bit is dropped from at least one of the sub-channels in an order based on the second power margin factors.

87. (New) The system of claim 86, wherein the order is an ascending order based on the value of the second power margin factor associated with each of the sub-channels.

88. (New) A system for transmitting data through sub-channels, comprising:

a memory to store signal-to-noise ratios associated with the sub-channels; and

a processor configured to

determine bit loading capacities and power modification factors associated with the sub-channels at the power margin; and

determine a total bit rate at the power margin according to the bit loading capacities.

89. (New) The system of claim 88, wherein the processor is configured to verify the bit loadings and the power modification factors at the power margin.

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90. (New) The system of claim 88, wherein the processor is configured to

determine an estimated power margin according to at least one of the total bit rate and a target bit rate;

replace the power margin with the estimated power margin; and

repeat a first loop of determining the bit loading capacities and the power modification factors, determining the total bit rate, determining the estimated power margin, and replacing the power margin, for a predetermined number of times, until the total bit rate approximates or equals to the target bit rate, or until obtaining two total bit rates that bound the target bit rate between the two total bit rates.

91. (New) The system of claim 90, when obtaining two total bit rates that bound the target bit rate between the two total bit rates, the processor is

to determine an updated power margin according to the two estimated power margins associated with the two total bit rates;

to replace the power margin with the updated power margin;

to repeat the first loop until obtaining the two total bit rates that bound the target bit rate, determining the updated power margin according to the two estimated power margins associated with the two total bit rates, and replacing the power margin with the updated power margin, for a predetermined number of times or until a most recent total bit rate equals to the target bit rate.

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92. (New) The system of claim 91, wherein the updated power margin is the square root of the multiplication of the two estimated power margins associated with the two total bit rates.

93. (New) The system of claim 88, wherein the processor is configured to determine the bit loading capacities and the power modification factors according to at least one of the signal-to-noise ratios, data rates associated with the sub-channels, number of sub-channels having a non-zero bit capacity, and a system transmission power.

94. (New) The system of claim 88, wherein the bit loading capacity of each sub-channel is represented by a minimum bit loading and a maximum bit loading.

95. (New) The system of claim 88, wherein each sub-channel has a minimum power modification factor and a maximum power modification factor respectively associated with the minimum bit loading and the maximum bit loading.

96. (New) The system of claim 88, wherein the processor is configured to determine whether to enable or disable at least one of the sub-channels according to the bit loadings and the power modification factors.

97. (New) A device to transmit data through sub-channels, comprising:

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circuitry to determine bit loading capacities and power modification factors associated with the sub-channels at the power margin; and

circuitry to determine a total bit rate at the power margin according to the bit loading capacities.

98. (New) The device of claim 97, further comprising

circuitry to determine an estimated power margin according to at least one of the total bit rate and a target bit rate;

circuitry to replace the power margin with the estimated power margin; and

circuitry to repeat a first loop of determining the bit loading capacities and the power modification factors, determining the total bit rate, determining the estimated power margin, and replacing the power margin, for a predetermined number of times, until the total bit rate approximates or equals to the target bit rate, or until obtaining two total bit rates that bound the target bit rate between the two total bit rates.

99. (New) A method for configuring a device to transmit data through sub-channels, comprising:

configuring the device to determine bit loading capacities and power modification factors associated with the sub-channels at the power margin; and

configuring the device to determine a total bit rate at the power margin according to the bit loading capacities.

100. (New) The method of claim 99, further comprising:

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